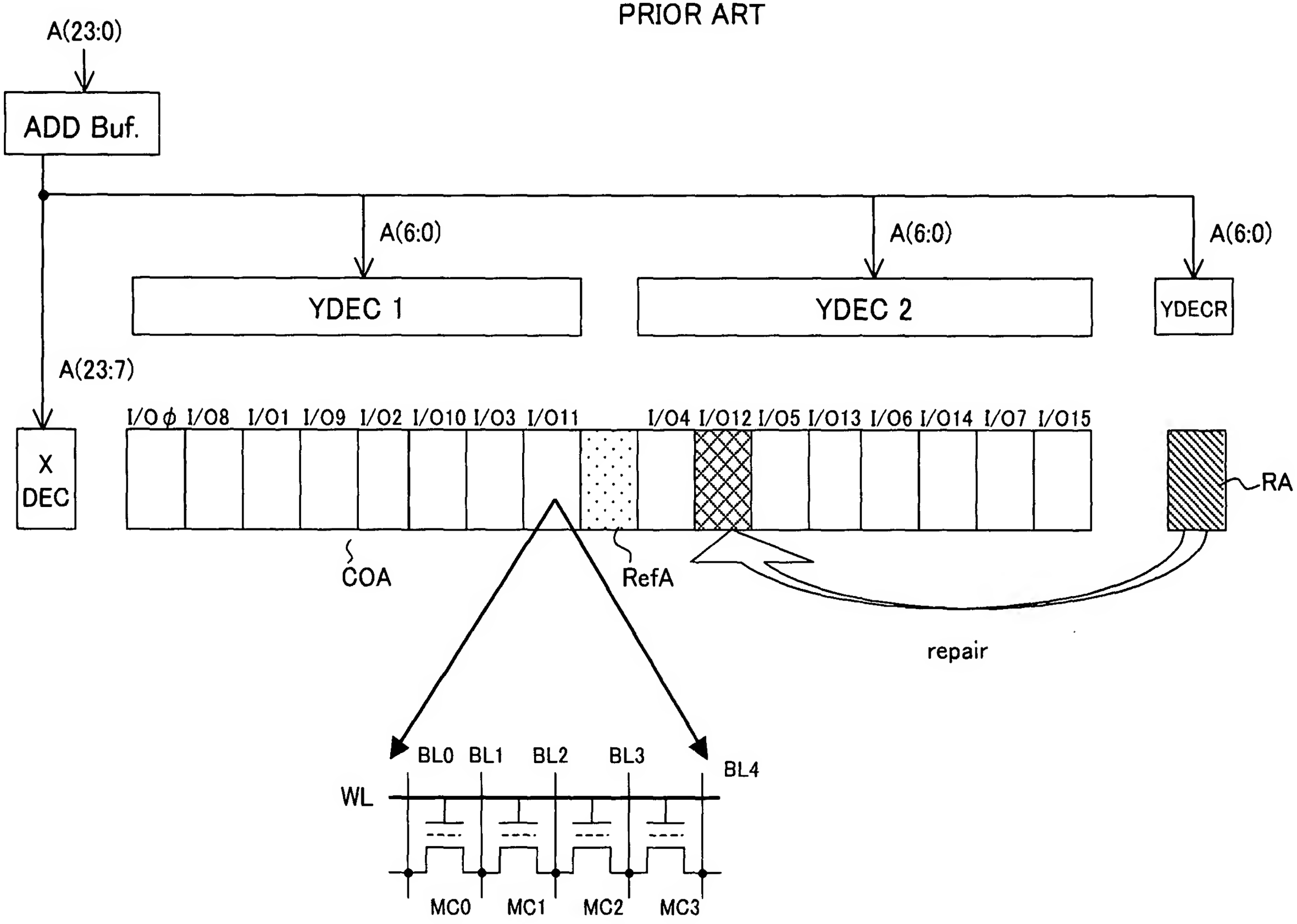
FIG. 1

PRIOR ART



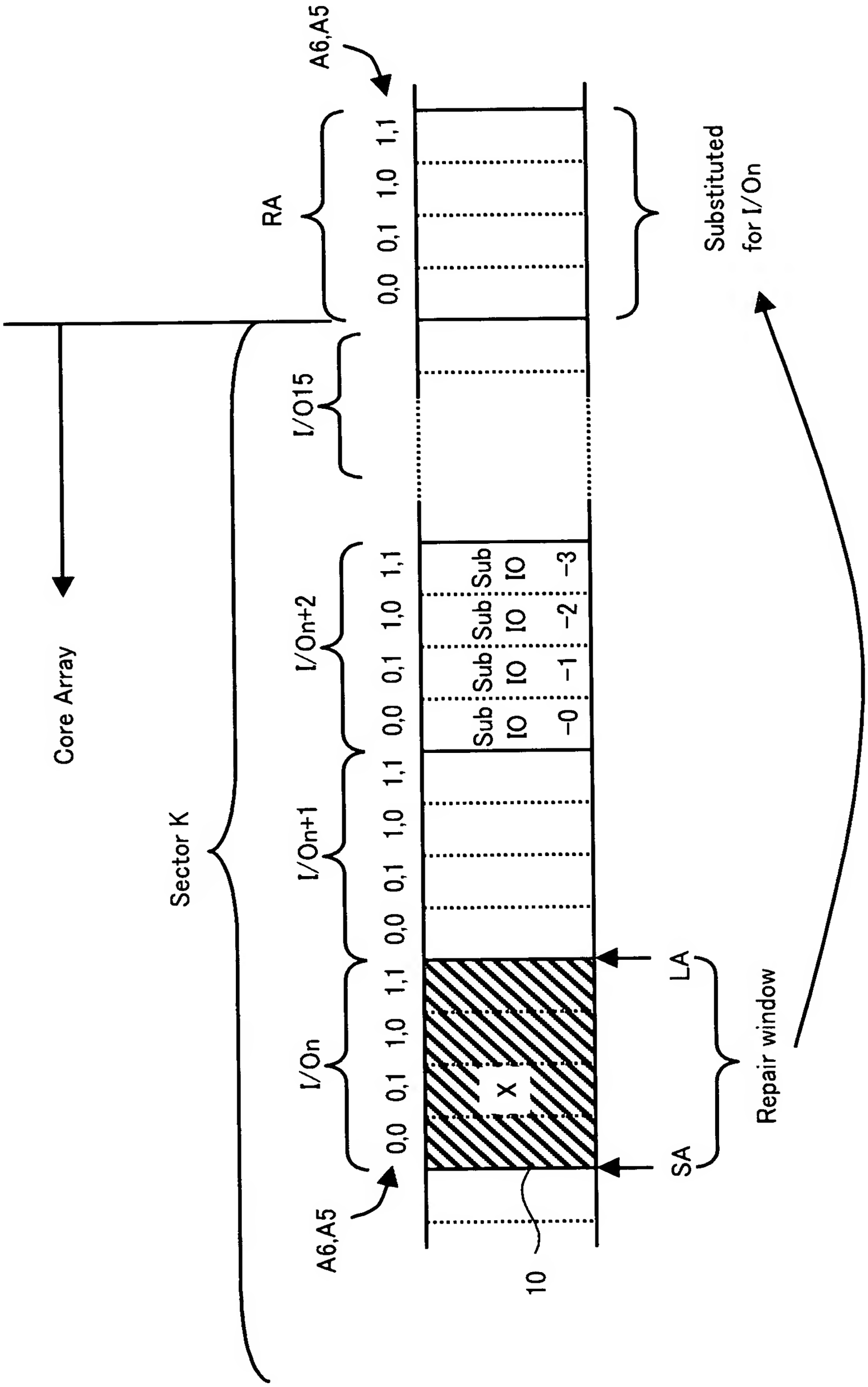

A6,A5
RA
0,0 0,1 1,0 1,1
Substituted
for I/On
I/O15
I/On+2
I/On+1
I/On
Sub IO -0
Sub IO -1
Sub IO -2
Sub IO -3
Sector K
Core Array
LA
SA
Repair window
X
10

FIG. 2

Title: Semiconductor Memory Enabling Correct Substitution of Redundant Cell Array
Inventor: Andy CHEUNG
Appln. No. : New Application
Docket No.: 108066-00101

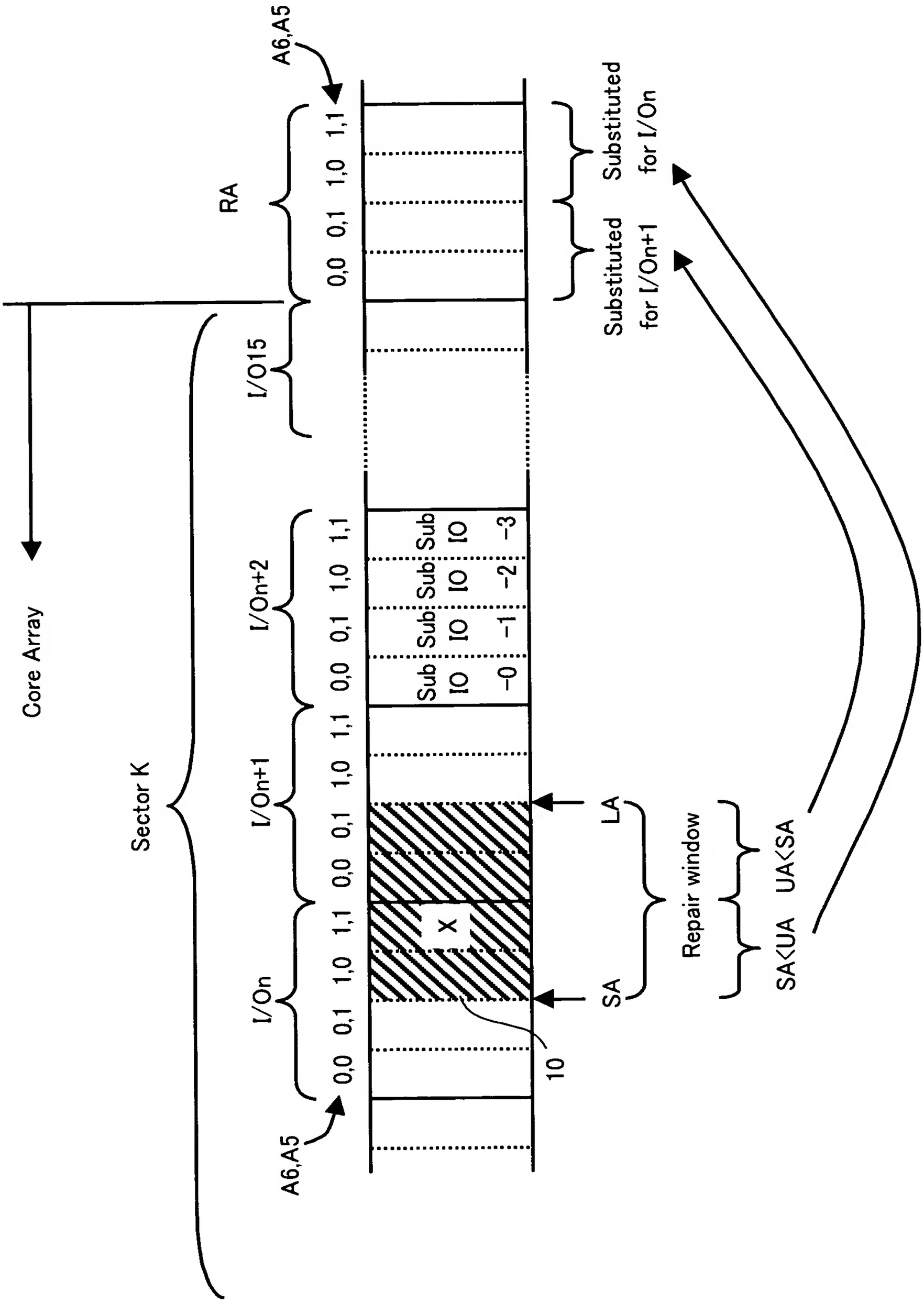


FIG. 3

Title: Semiconductor Memory Enabling Correct
Substitution of Redundant Cell Array
Inventor: Andy CHEUNG
Appln. No. : New Application
Docket No.: 108066-00101

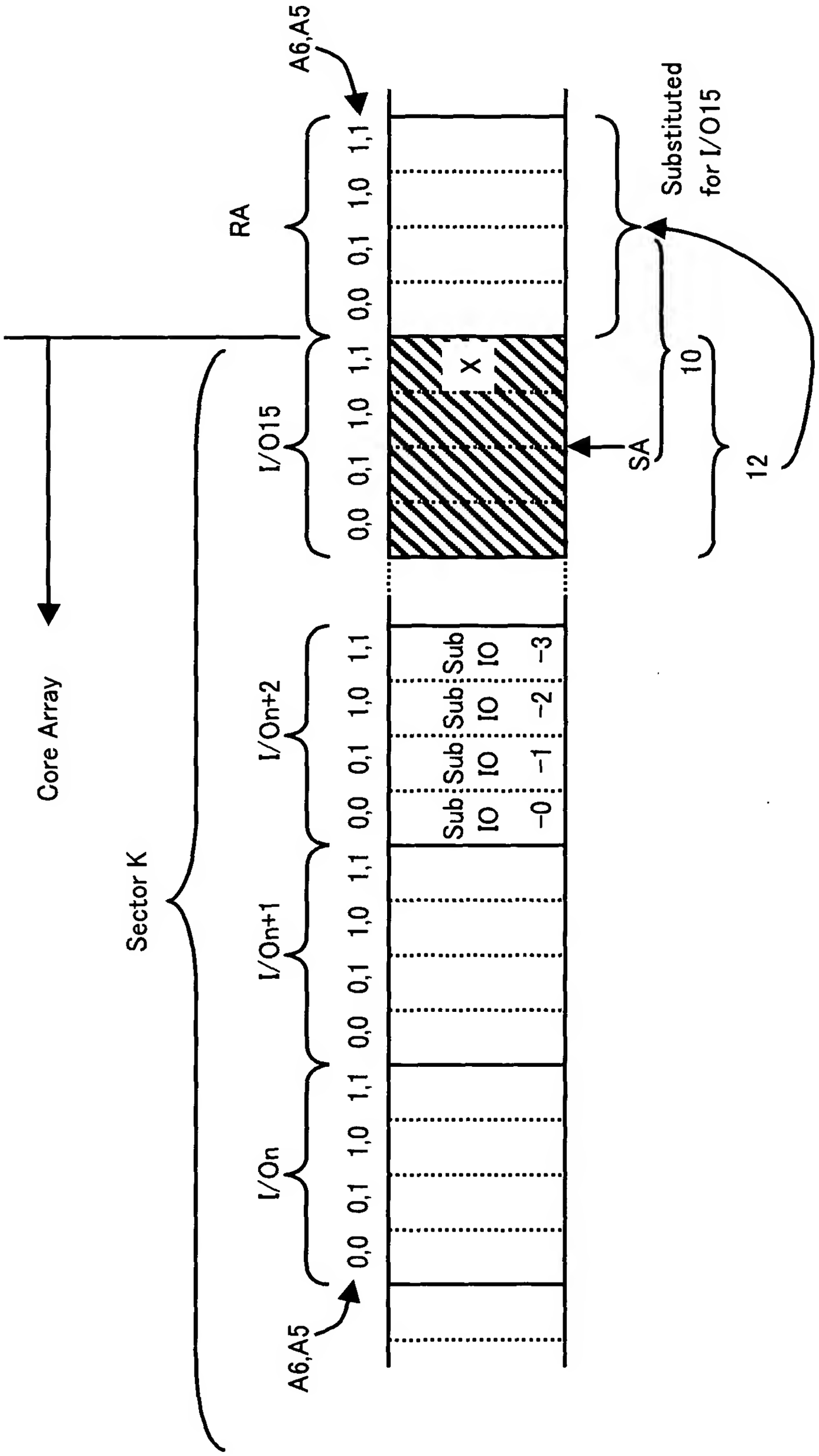


FIG. 4

Title: Semiconductor Memory Enabling Correct Substitution of Redundant Cell Array
Inventor: Andy CHEUNG
Appln. No. : New Application
Docket No.: 108066-00101

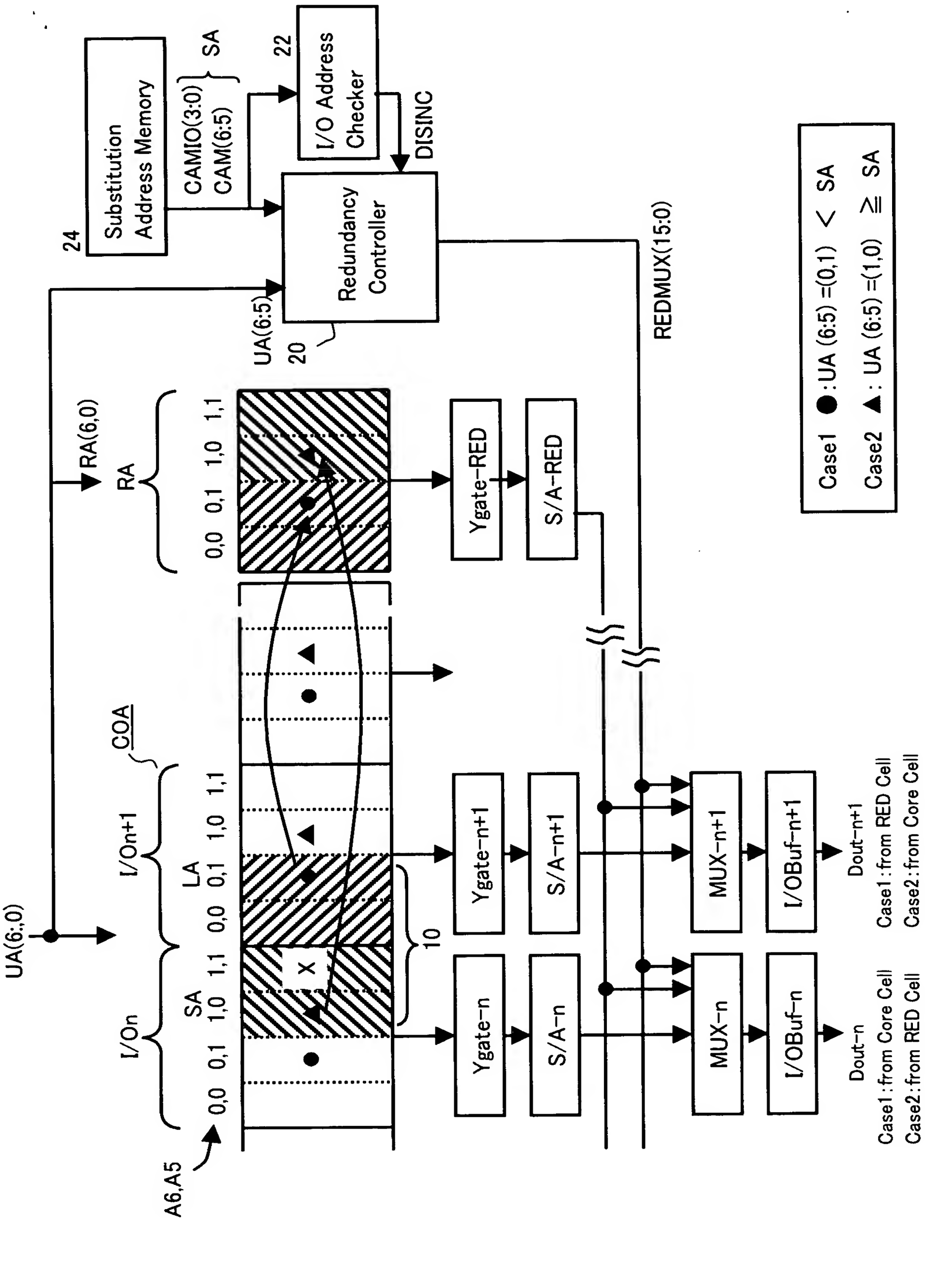
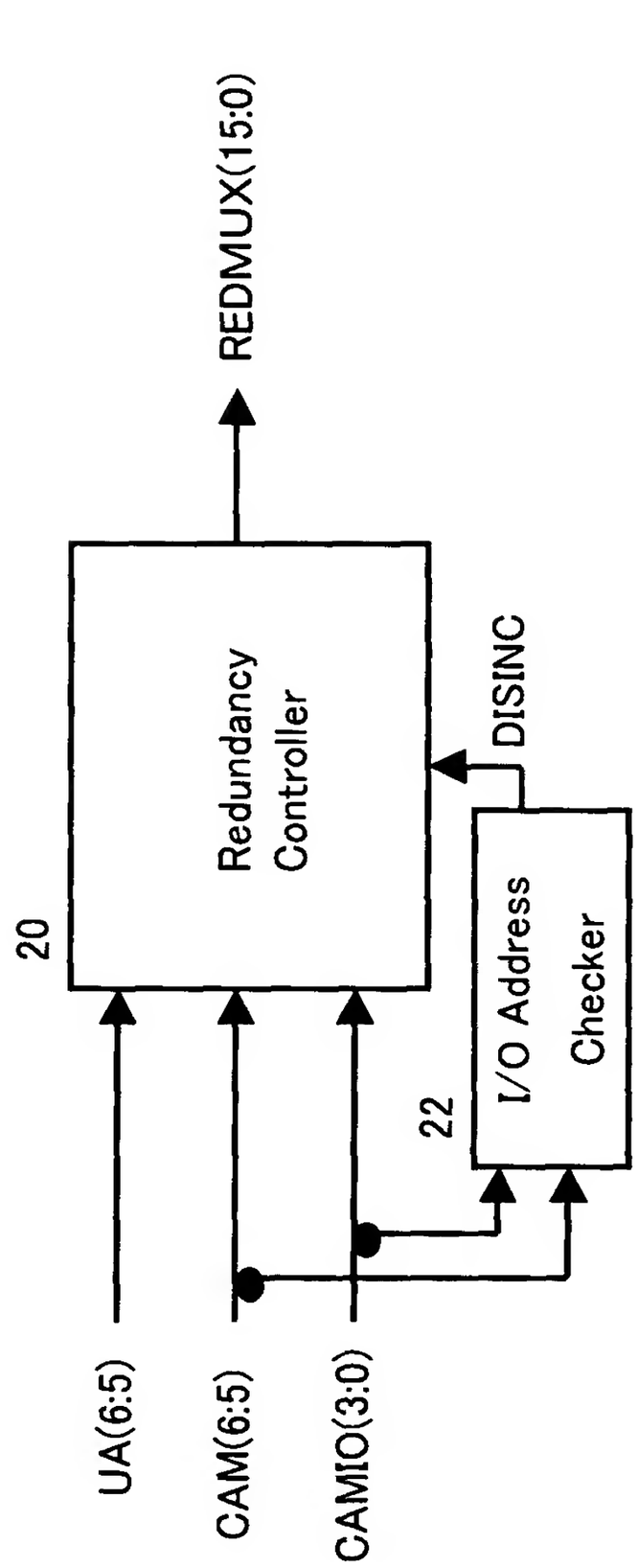


FIG. 5


UA(6:5)
CAM(6:5)
CAMIO(3:0)
20
Redundancy Controller
22
I/O Address Checker
DISINC
REDMUX(15:0)

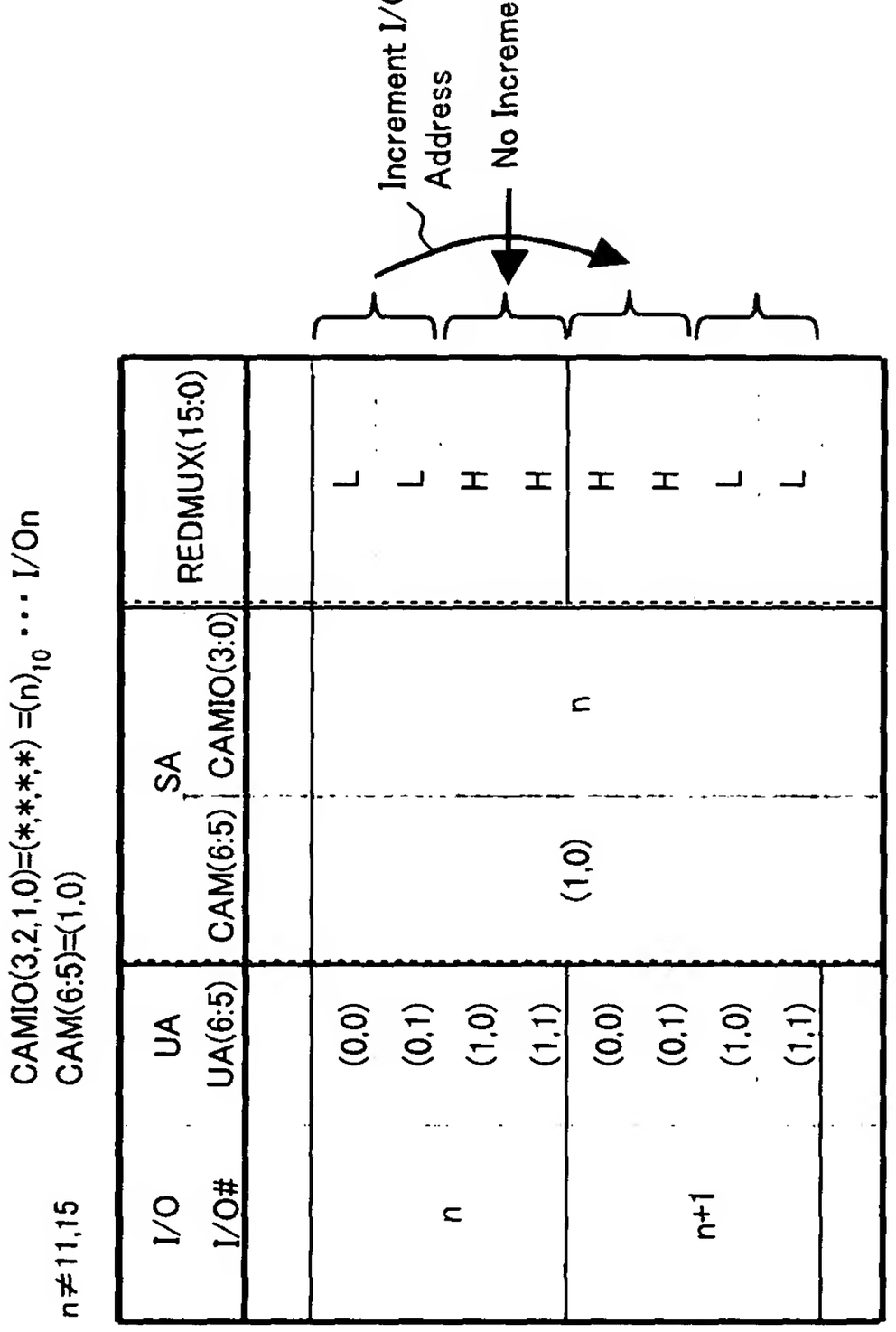
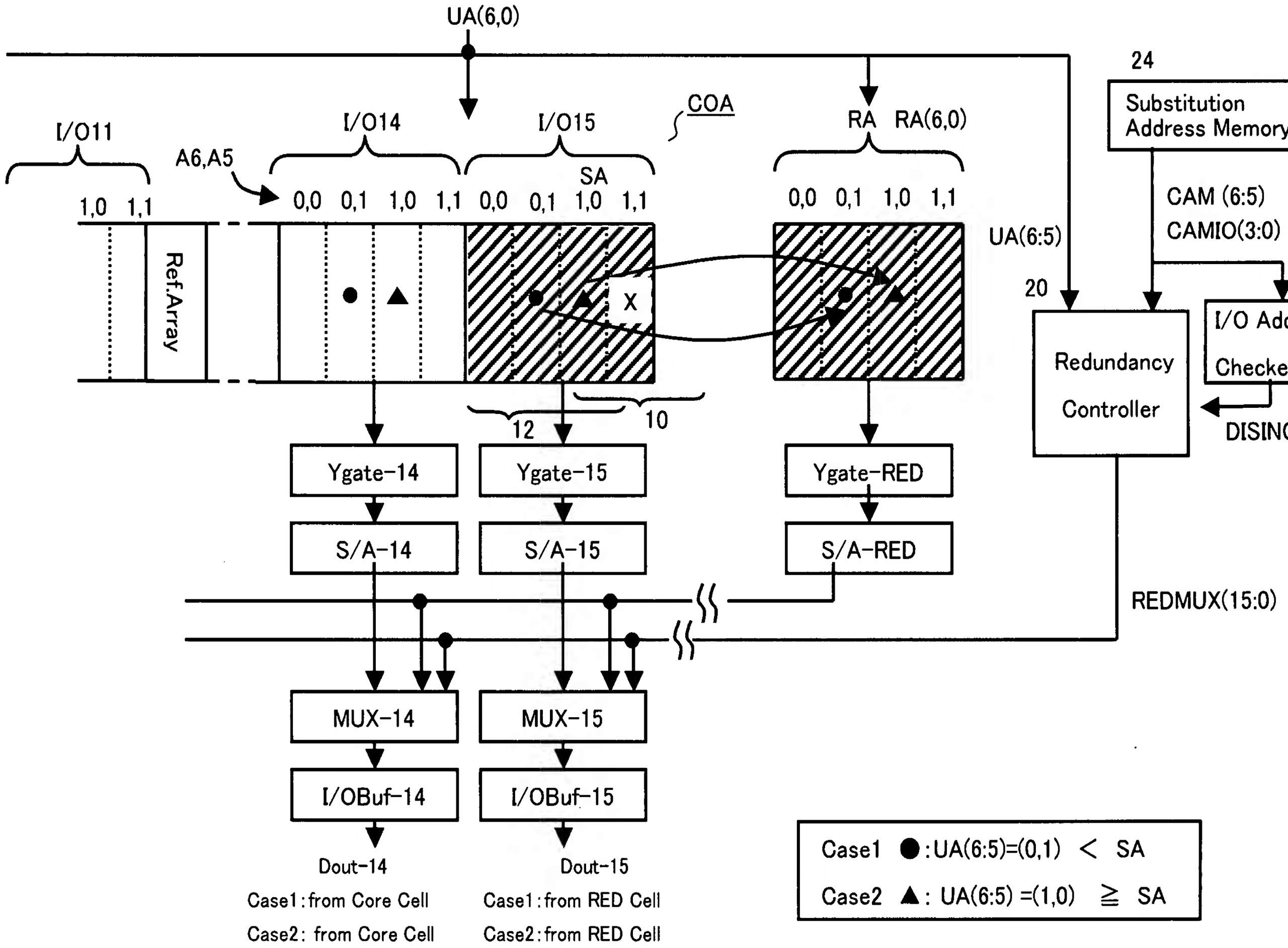

CAMIO(3,2,1,0)=(*,*,*,*) =(n)10 ··· I/On
CAM(6:5)=(1,0)
UA
UA(6:5)
SA
CAM(6:5)
CAMIO(3:0)
REDMUX(15:0)
(0,0)
(0,1)
(1,0)
(1,1)
(1,0)
n
L
H
Increment I/O block Address
No Increment
n≠11,15
I/O
I/O#
n
n+1

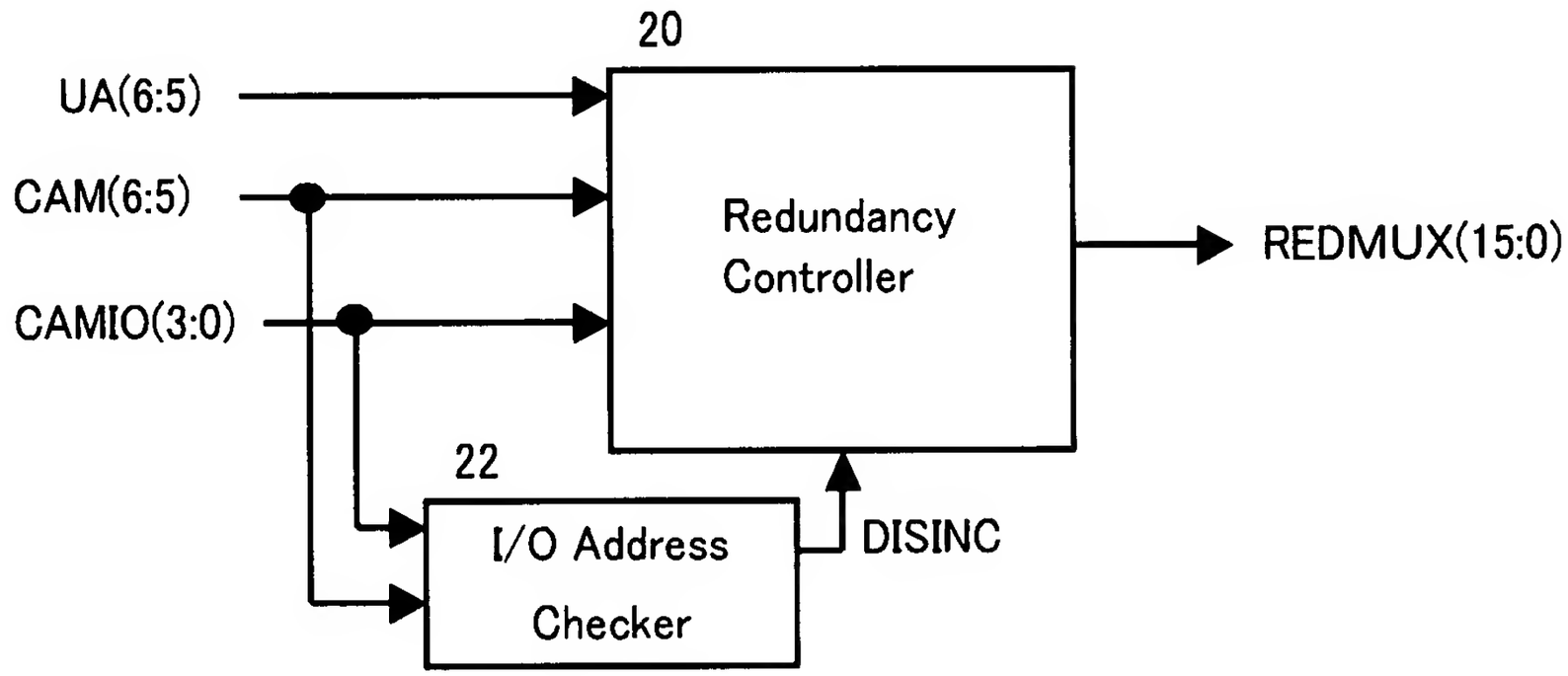
FIG. 6

FIG. 7



Title: Semiconductor Memory Enabling Correct Substitution of Redundant Cell Array
Inventor: Andy CHEUNG
Appln. No. : New Application
Docket No.: 108066-00101

FIG. 8



CAMIO(3,2,1,0)=(1,1,1,1) =$(15)_{10}$ ··· I/O15
CAM(6:5)=(1,0)

I/O I/O#	UA UA(6:5)	SA CAM(6:5)	SA CAMIO(3:0)	REDMUX(15:0)
14	(0,0)	(1,0)	15	L
	(0,1)			L
	(1,0)			L
	(1,1)			L
15	(0,0)			H
	(0,1)			H
	(1,0)			H
	(1,1)			H

Inhibit I/O Increment

Title: Semiconductor Memory Enabling Correct Substitution of Redundant Cell Array
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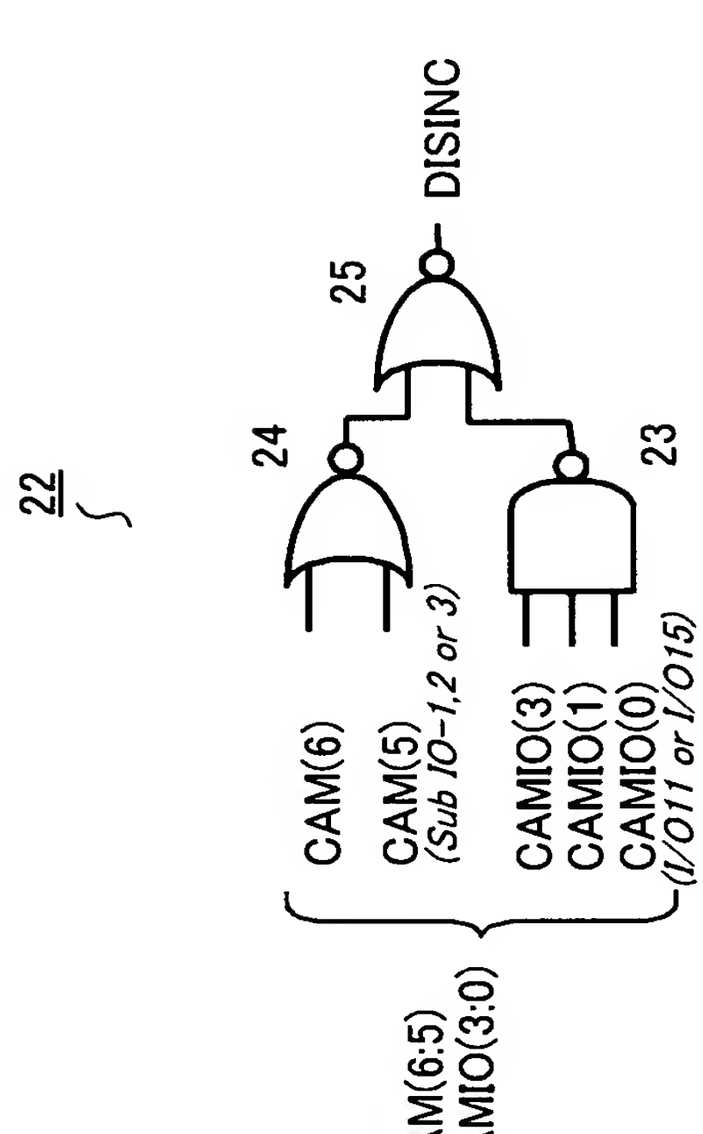
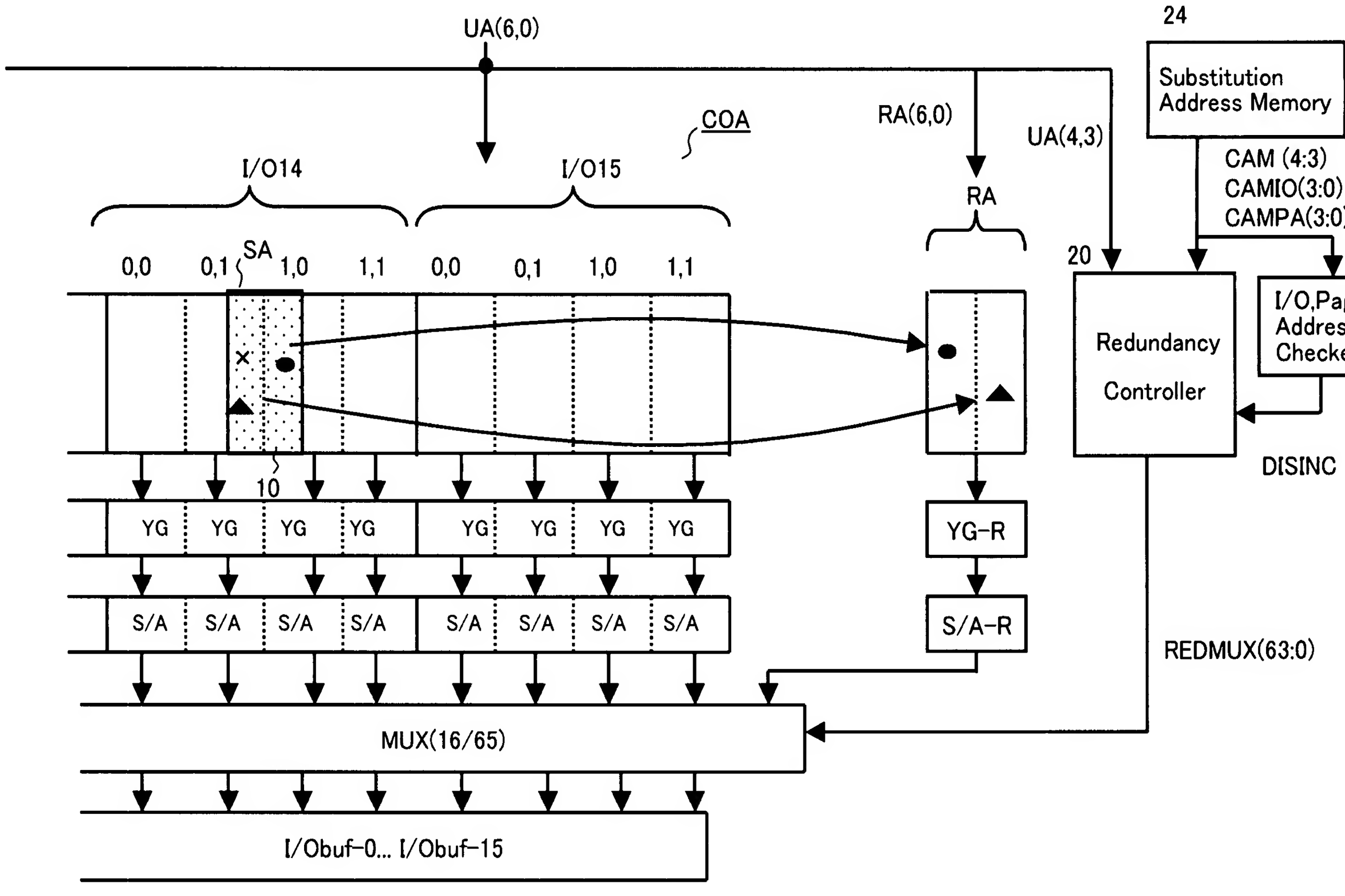


I/O Address Checker Circuit

FIG. 9

FIG. 10



Title: Semiconductor Memory Enabling Correct Substitution of Redundant Cell Array
Inventor: Andy CHEUNG
Appln. No.: New Application
Docket No.: 108066-00101

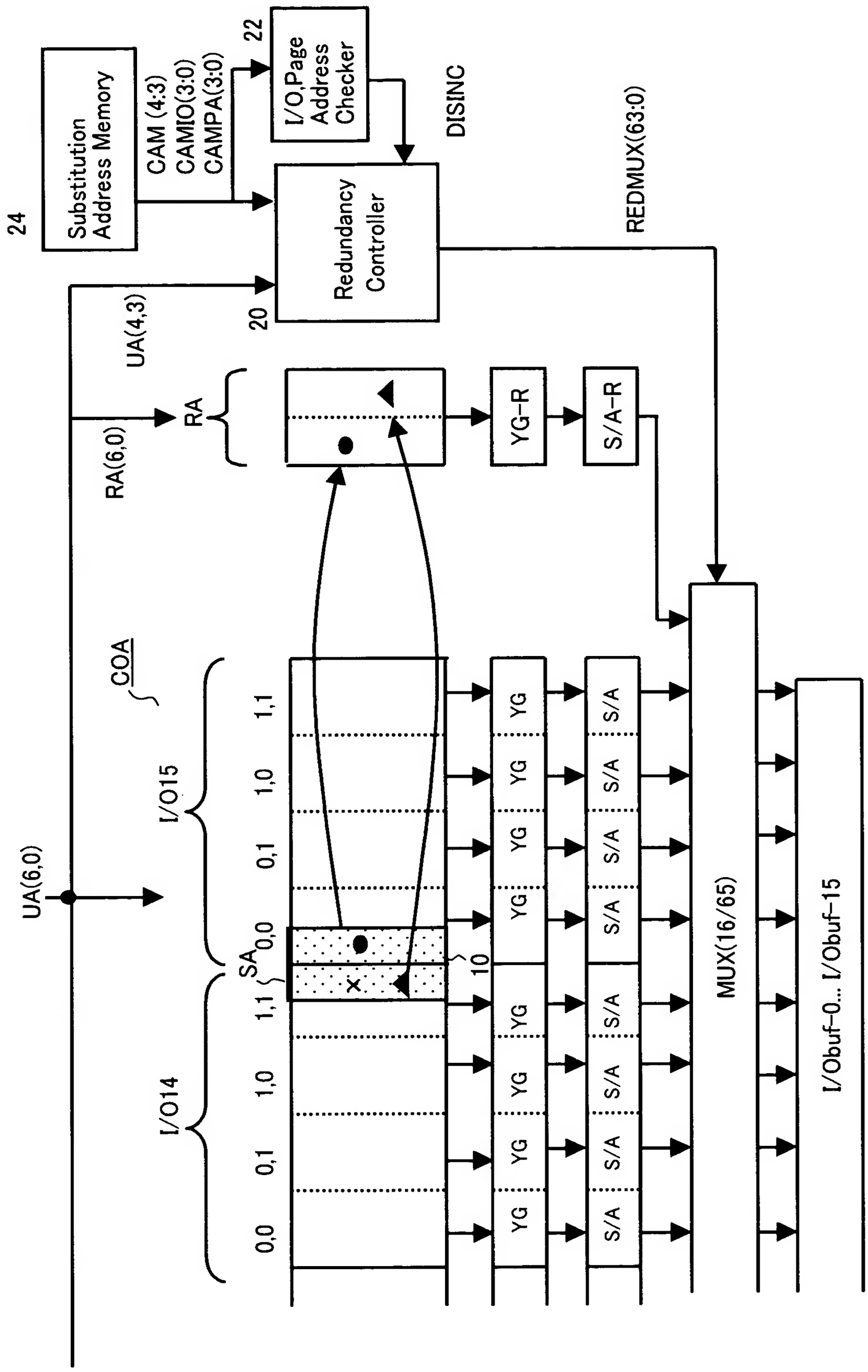
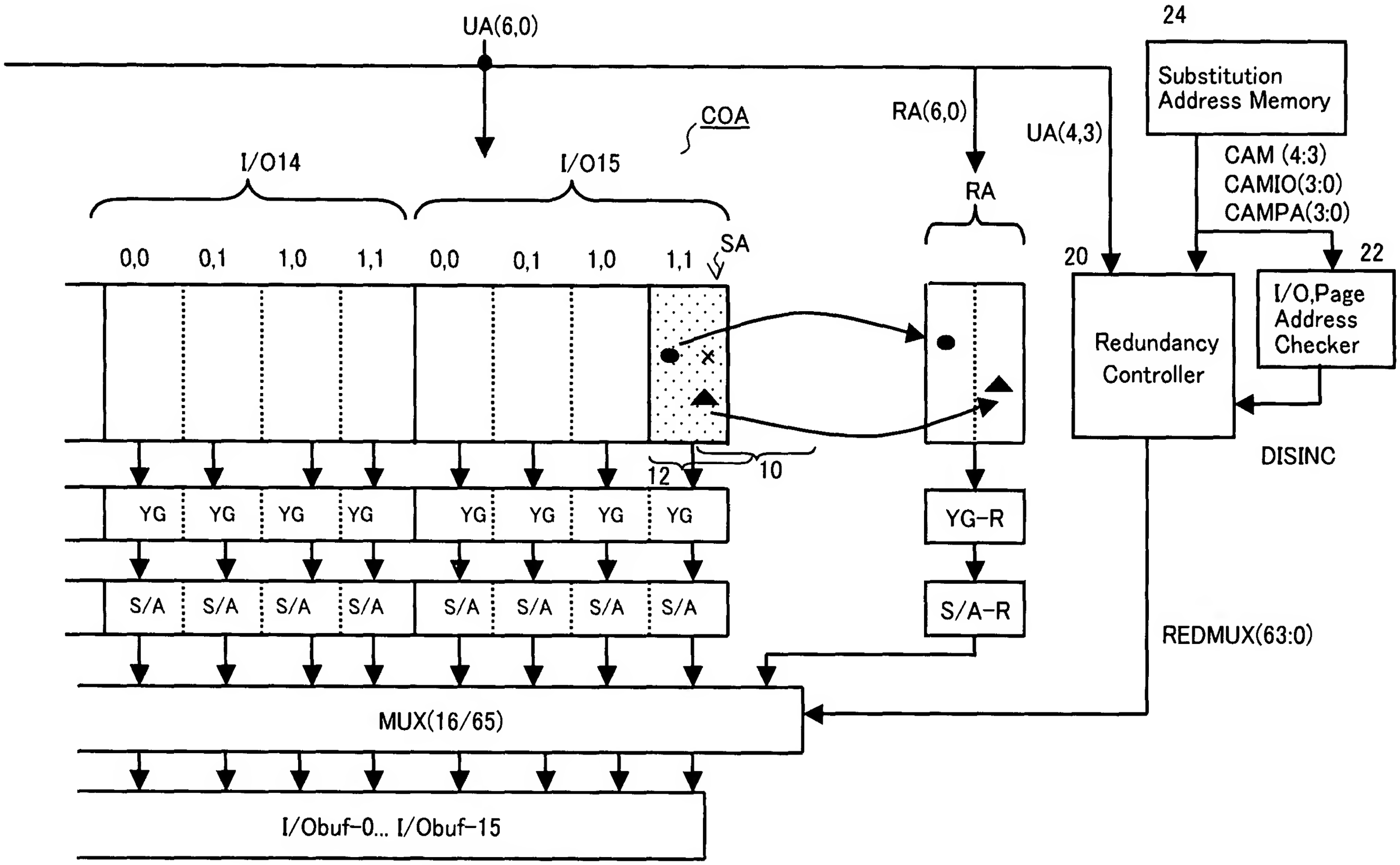

24
Substitution Address Memory
CAM (4:3)
CAMIO(3:0)
CAMPA(3:0)
22
I/O,Page Address Checker
DISINC
REDMUX(63:0)
20
Redundancy Controller
UA(4,3)
RA(6,0)
RA
YG-R
S/A-R
COA
UA(6,0)
I/O15
I/O14
SA0,0
1,1
0,1
1,0
1,1
10
YG
S/A
MUX(16/65)
I/Obuf-15
I/Obuf-0...

FIG. 11

FIG. 12



Title: Semiconductor Memory Enabling Correct Substitution of Redundant Cell Array
Inventor: Andy CHEUNG
Appln. No.: New Application
Docket No.: 108066-00101

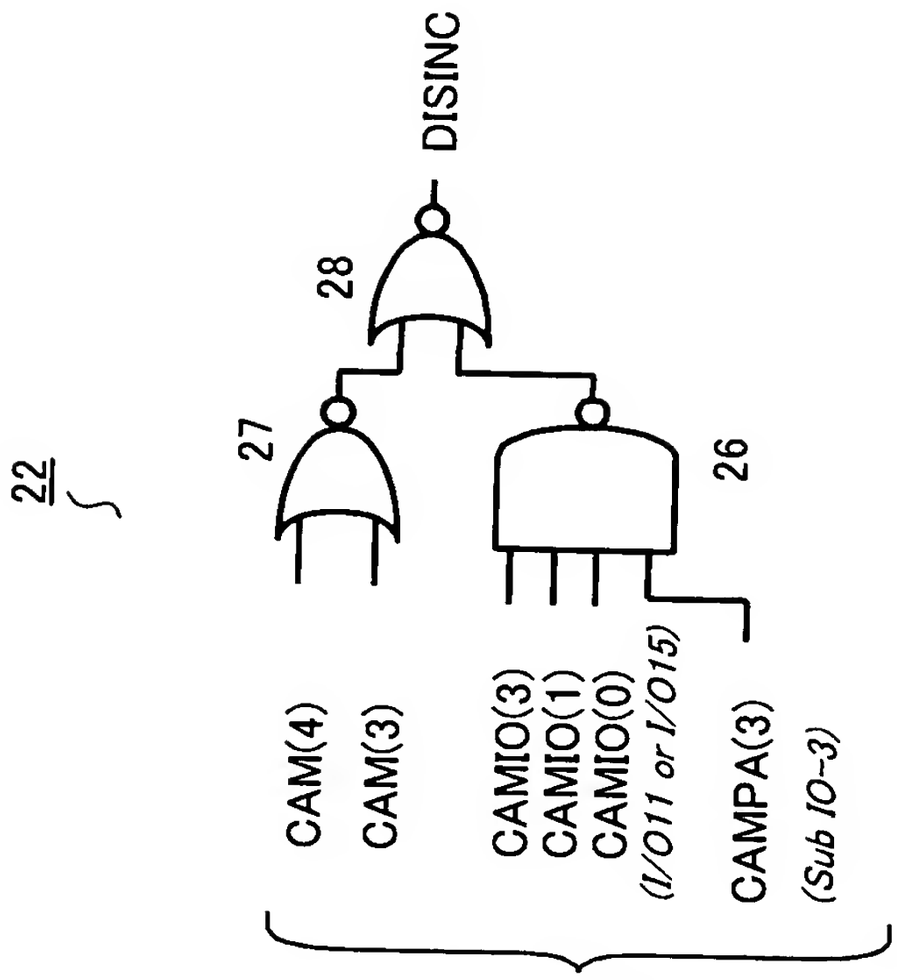

22
27
28
DISINC
CAM(4)
CAM(3)
CAMIO(3)
CAMIO(1)
CAMIO(0)
(I/O11 or I/O15)
CAMPA(3)
(Sub IO-3)
26
I/O,Page Address Checker Circuit
CAM(4:3)
CAMIO(3:0)
CAMPA(3:0)

FIG. 13